WHAT IS CLAIMED IS:

1. An SLM (Selected Mapping) apparatus for converting a signal block including a plurality of signals corresponding to a plurality of sub-carriers contained in a frequency domain for use in a transmitter of an OFDM (Orthogonal Frequency Division Multiplexing) communication system into a plurality of signal sequences contained in a time domain, and selecting a signal sequence having a lowest PAPR (Peak-to-Average Power Ratio) among the converted signal sequences, the SLM apparatus comprising:

a single IFFT (Inverse Fast Fourier Transformer) for performing an Inverse Fast Fourier Transform process on the plurality of signals of the signal block and generating a conversion sequence symbol having a plurality of samples;

a shift register for storing the plurality samples of the conversion sequence symbol generated from the IFFT,

a plurality of multiplier groups each including a plurality of multipliers, and

a plurality of adder groups each having an adder for adding up output values of the plurality of multipliers included in each of the plurality of multiplier groups;

wherein the shift register includes a plurality of memories serially connected to each other for storing individual samples and acts as a cyclic shift register for connecting an output terminal of a last memory among the memories to an input terminal of a first memory among the memories, such that a first input sample among the individual samples is applied to the first memory when it is generated from the last memory; and

wherein the plurality of multipliers are each connected to output terminals

of the plurality of memories, receive a plurality of mask coefficient groups, each including mask coefficients for generating a plurality of signal sequences containing a signal sequence having the lowest PAPR, and multiply output values of the plurality of memories by another received mask coefficient group among the received plurality of mask coefficient groups, whenever the individual samples of the shift register are circulated.

2. The apparatus as set forth in claim 1, further comprising:

a selector for selecting a specific signal sequence having a lowest PAPR among a plurality of signal sequences that are generated from the plurality of adder groups each having an adder for adding up output values of the plurality of multipliers.

3. The apparatus as set forth in claim 1, further comprising a mask generator for generating the plurality of mask coefficient groups.

4. The apparatus as set forth in claim 1, wherein the mask coefficients are determined by:

$$c_{p,q} = \frac{1}{N}\sum_{i=0}^{N-1} m_{p,i} \cdot e^{j(2\pi/N)\cdot i\cdot q}$$

where $c_{p,q}$ is a q-th coefficient of a mask operation matrix determined by a p-th mask sequence, N is a magnitude of the signal block, $m_{p,i}$ is an i-th bit of the p-th mask sequence, and e is a natural logarithm.

5. The apparatus as set forth in claim 1, wherein the plurality of multiplier groups share output terminals of the shift register.

6. An SLM (Selected Mapping) method for converting a signal block including a plurality of signals corresponding to a plurality of sub-carriers contained in a frequency domain for use in a transmitter of an OFDM (Orthogonal Frequency Division Multiplexing) communication system into a plurality of signal sequences contained in a time domain, and selecting a signal sequence having a lowest PAPR (Peak-to-Average Power Ratio) among the converted signal sequences, the SLM method comprising the steps of:

a) performing an Inverse Fast Fourier Transform (IFFT) process on the plurality of signals included in the signal block, and generating a conversion sequence symbol having a plurality of samples;

b) storing the plurality of samples of the IFFT-processed conversion sequence symbol in a shift register, wherein the shift register includes a plurality of memories, which are serially connected to each other, for storing individual samples, and acts as a cyclic shift register for connecting an output terminal of a last memory among the plurality of memories to an input terminal of a first memory among the plurality of memories such that a first input sample among the plurality of samples is applied to the first memory whenever it is generated from the last memory;

c) connecting a plurality of multiplier groups, each including a plurality of multipliers, to output terminals of the plurality of memories;

d) receiving in the plurality of multipliers, a plurality of mask coefficient groups, each including mask coefficients, for generating a plurality of signal sequences containing a signal sequence having the lowest PAPR;

e) multiplying output values of the plurality of memories by another received mask coefficient group among the received plurality of mask coefficient groups, whenever the plurality of samples of the shift register are circulated; and

f) adding up output values of the plurality of multipliers contained in each of the plurality of multiplier groups.

7. The method as set forth in claim 6, further comprising the step of:

g) selecting a specific signal sequence having the lowest PAPR among a plurality of signal sequences that are generated from the plurality of adder groups each having an adder for adding up output values of the plurality of multipliers.

8. The method as set forth in claim 6, wherein the plurality of mask coefficient groups are generated by a predetermined mask generator.

9. The method as set forth in claim 6, wherein the plurality of mask coefficients are determined by

$$c_{p,q} = \frac{1}{N}\sum_{i=0}^{N-1} m_{p,i} \cdot e^{j(2\pi/N)\cdot i\cdot q}$$

where $c_{p,q}$ is a q-th coefficient of a mask operation matrix determined by a p-th mask sequence, N is a magnitude of the signal block, $m_{p,i}$ is an i-th bit of the p-th mask sequence, and e is a natural logarithm.

10. The method as set forth in claim 6, wherein the plurality of multiplier groups share output terminals of the shift register.

11. A transmitter apparatus for converting a signal block including a plurality of signals corresponding to a plurality of sub-carriers contained in a frequency domain for use in a transmitter of an OFDM (Orthogonal Frequency Division Multiplexing) communication system into a plurality of signal

sequences contained in a time domain, selecting a signal sequence having a lowest PAPR (Peak-to-Average Power Ratio) among the converted signal sequences, and transmitting the selected signal sequence, the transmitter apparatus comprising:

a single IFFT (Inverse Fast Fourier Transformer) for performing an Inverse Fast Fourier Transform process on the plurality of signals of the signal block, and generating a conversion sequence symbol having a plurality of samples;

a mask operator for receiving a plurality of mask coefficient groups for generating a plurality of signal sequences containing a signal sequence having a lowest PAPR, multiplying the plurality of samples by another received mask coefficient group among the received plurality of mask coefficient groups, whenever the plurality of samples generated from the IFFT are circulated, and generating a plurality of masking-processed sequences; and

a selector for selecting a specific sequence having a lowest PAPR among the masking-processed sequences generated from the mask operator, and transmitting the selected sequence.

12. The apparatus as set forth in claim 11, wherein the mask operator further includes a shift register for storing the plurality of samples generated from the IFFT.

13. The apparatus as set forth in claim 12, wherein the shift register includes a plurality of memories serially connected to each other for storing individual samples, respectively.

14. The apparatus as set forth in claim 13, wherein the shift register

acts as a cyclic shift register for connecting an output terminal of a last memory among the plurality of memories to an input terminal of a first memory among the plurality of memories, such that a first input sample among the plurality of samples is applied to the first memory whenever it is generated from the last memory.

15. The apparatus as set forth in claim 11, wherein the mask operator further includes a plurality of multiplier groups, each including a plurality of multipliers, wherein the plurality of multipliers are each connected to output terminals of the plurality of memories, receive the plurality of mask coefficient groups, each including plurality of mask coefficients for generating a plurality of signal sequences including a signal sequence having a lowest PAPR, and multiply the plurality of samples by another received mask coefficient group among the received plurality of mask coefficient groups, whenever the plurality of samples of the shift register are circulated.

16. The apparatus as set forth in claim 11, wherein the mask operator further includes a plurality of adder groups, each having an adder for adding up output values of the plurality of multipliers contained in each of the plurality of multiplier groups.

17. The apparatus as set forth in claim 11, further comprising:

a channel encoder for performing a channel-encoding process on an information bit to be transmitted.

18. The apparatus as set forth in claim 17, further comprising:

a mapper for controlling the information bit generated from the channel

encoder to be associated with a signal contained in a predetermined signal constellation.

19. A data transmission method for converting a signal block including a plurality of signals corresponding to a plurality of sub-carriers contained in a frequency domain for use in a transmitter of an OFDM (Orthogonal Frequency Division Multiplexing) communication system into a plurality of signal sequences contained in a time domain, selecting a signal sequence having a lowest PAPR (Peak-to-Average Power Ratio) among the converted signal sequences, and transmitting the selected signal sequence, the method comprising the steps of:

a) performing an Inverse Fast Fourier Transform (IFFT) process on the signals of the signal block, and generating a conversion sequence symbol having a plurality of samples;

b) receiving a plurality of mask coefficient groups for generating a plurality of signal sequences containing a signal sequence having a lowest PAPR, multiplying the plurality of samples by another received mask coefficient group among the received plurality of mask coefficient groups, whenever the plurality of samples generated from the IFFT are circulated, and generating a plurality of masking-processed sequences; and

c) selecting a specific sequence having a lowest PAPR among the plurality of masking-processed sequences, and transmitting the selected sequence.

20. The method as set forth in claim 19, further comprising the step of:

d) storing the plurality of samples generated by the IFFT process in a predetermined shift register, which includes a plurality of memories connected in

series to each other.

21. The method as set forth in claim 20, wherein the shift register acts as a cyclic shift register for connecting an output terminal of a last memory among the plurality of memories to an input terminal of a first memory among the plurality of memories, such that a first input sample among the plurality of samples is applied to the first memory when it is generated from the last memory.

22. The method as set forth in claim 19, wherein the step (b) comprises the step of:

b1) connecting a plurality of multipliers to output terminals of plurality of memories, receiving the plurality of mask coefficient groups, each including a plurality of mask coefficients, for generating the plurality of signal sequences containing the signal sequence having the lowest PAPR, and multiplying the plurality of samples by another received mask coefficient group among the received plurality of mask coefficient groups, when the plurality of samples of the shift register are circulated.

23. The method as set forth in claim 19, wherein the step (b) further comprises the step of:

b2) adding up output values of multiplication processes of each of the plurality of mask coefficient groups.